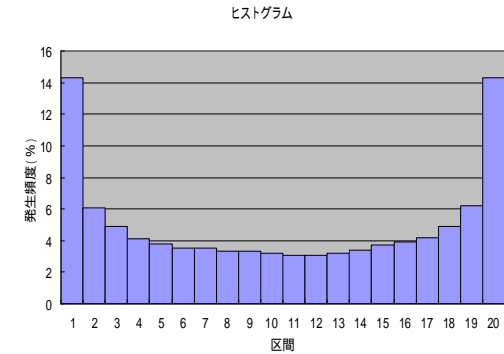
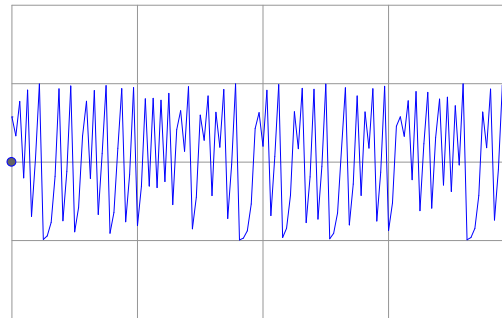


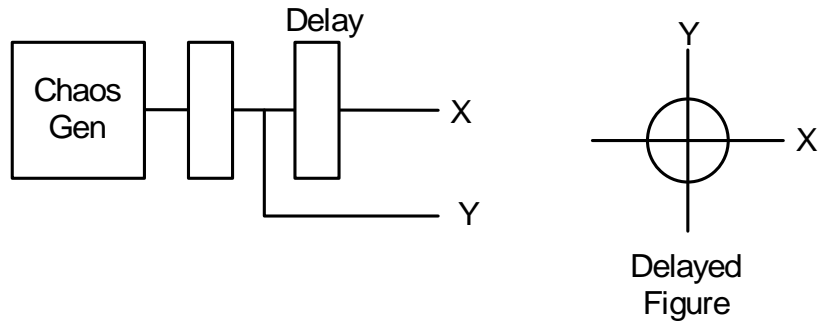
Chaos code of the Logistic Map

$$X_{n+1} = aX_n(1 - X_n)$$

$$a = 4 \quad 0 \leq X_n \leq 1$$

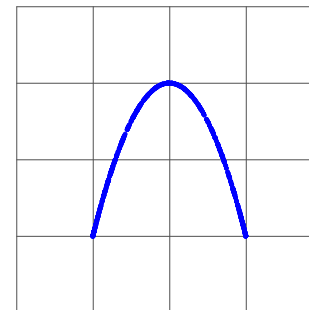


FPGA構成

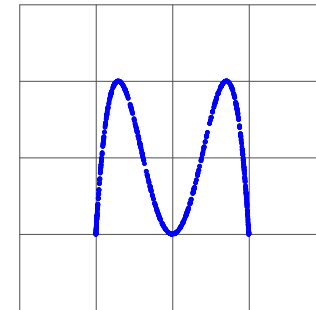


(Two-dimensional phase diagrams)

Delayed Lissajous Figure(Return Map)



Delay 1



Delay 2

FPGA implementation

File Name: ChaosDLY\_15.rbt

## Signals

Port	Signals
0	Chaos Delay #1
1	Chaos Delay #2
2	Chaos Delay #3
3	Chaos Delay #4
4	Chaos Delay #5